REMARKS

This is in full and timely response to the above-identified Office Action. Reexamination and reconsideration in light of the proposed amendments and the following remarks are respectfully requested.

Interview Summary – by Applicant

For the Patent Office: - Examiner Khanh DANG

For the Applicant(s): – Keith Townsend (Patent Agent)

Time: Thursday 07/08/04

At the interview, the applicant basic premise as to what was being sought to be claimed, was explained. The feature that the interrupt was induced at preset intervals and run for a preset time was discussed and the manner in which the interrupt in the first reference could not meet this requirement was advanced. It was agreed that the OR gate 7 of Hayashi was an interrupt trigger generating means but this did not negate the fact that claim 7 recited interrupts being made for predetermined time and a predetermined intervals. The Examiner expressed agreement.

The fact that the claims called for three different memories and that Hayashi only disclosed two, was discussed. The Examiner noted this point. The fact that the rejections did not identify where each of the elements, that are recited in at least claims 7 and 8, could be found in each of the references, was briefly discussed and the Examiner expressed recognition of this issue.

The cyclic nature of the routine disclosed in Fig. 29 of Yonezawa was discussed. It was pointed out that even though this routine showed a cyclic pattern that there was no disclosure that the duration of each of the steps were each always of the same duration. Thus, even though it showed input/output refresh processing there was not disclosure which would suggest that this anticipated the claimed subject matter. The Examiner agreed and the meaning of what would be understood by the claimed term of "cyclic" as different from the fixed time/fixed interval was discussed.

The basis for the Examiner's holding under 35 USC § 112 that the claimed elements were insufficiently recited in the claims to provide the necessary nexus therebetween, was discussed. It was pointed out that a careful review of the claims would reveal that each of the elements was interconnected by after recited limitations. The Examiner pressed for suggestions as to what limitations might be added to render the claims clear and definite. The Examiner did not specify any examples of where insufficient nexus was deemed to occur in the claims.

The Examiner closed the interview with a promise to work with the Applicants and that he would issue an interview summary in the near future.

Interview Summary from PTO

The Interview Summary that should have been issued by the Patent Office has not been received by the Applicant's representatives as of August 16, 2004. It is respectfully requested that every effort be made to ensure that this document is mailed to the Applicant's representatives as soon as practicable. Applicant' s representative has been informed that the art group is being moved and that the Interview Summary was in the process of being scanned into the electronic record and that this was the cause of the delay.

Rejections under 35 USC § 112

The rejection of claims 2-5 and 7-8 under 35 USC § 112, second paragraph, as being indefinite in that "the essential structural cooperative relationship between elements recited in the claims have been omitted, such omission amounting to a gap between the necessary structural connections." In traverse, it is submitted that adequate cooperative relationship is set forth in the claims and that with a careful reading this relationship can be determined. Reconsideration and withdrawal of this rejection is courteously solicited.

Claim Amendments

In this response, independent claims 7 and 8 have amended to clarify that the user program process and I/O refresh process are executed by the microprocessor according to the normal procedure for a first prescribed constant amount of time, and

the peripheral service process is executed at prescribed constant intervals for a second prescribed constant amount of time. It is submitted that this clarifies over the art of record and places the claims in allowable form as will be appreciated from the following remarks relating to each of the four references which are applied under 35 USC § 102. For these reasons, it is respectfully requested that the proposed amendments be entered.

It is submitted that the amendments do not introduce any new matter or raise any issues that would require a further search or consideration. That is to say, it is merely a clarification that – if the interrupts occur at prescribed (and therefore constant) intervals and if the amount of time for which the peripheral service process is carried out, is prescribed (and therefore also constant) – that the period for which the peripheral service process and the period for which the user program process and I/O refresh process are executed, will be both constant. In that the two periods are different pertains to the above-mentioned clarification over the cited references.

Rejections under 35 USC § 102

1) The rejection of claims 2-5 and 7-8 under 35 USC § 102(b) as being anticipated by Hayashi is respectfully traversed.

Rejections under the 35 USC § 102 statute, are based on the premise that to anticipate a claim, each and every element of the claim must be shown in a single reference. When a claimed element cannot be found in the reference, the reference does not anticipate the claimed invention. Further, it is incumbent upon the Examiner to identify in the rejection where in the reference each element may be found. Ex parte Levy, 17 U.S.P.Q.2d 1461 (Bd. Pat. App. Intrf. 1990). Consequently, when a rejection fails to identify a claimed element, the rejection fails to establish a *prima facie* case of anticipation.

The independent claims 7 and 8 recite three memories. That is to say, these claims each recite an I/O memory for storing I/O data corresponding to the I/O unit; a user program memory for storing user program corresponding to user defined control requirements; and a system program memory for storing various system programs.

In this rejection, none of the three claimed memories are specifically identified and there is no indication as to where they are disclosed in the cited reference. It is respectfully submitted that the rejection is untenable for at least this reason. Indeed, is it submitted that Hayashi discloses only two memories – common memory 2e and control memory 2b.

While the OR circuit can be broadly considered to be an interrupt trigger generating means, it is the Applicant's position that the command execution process is not constant and as long as the interruption triggers are generated according to the input signals of the PLC, the interruption triggers will not be generated at prescribed intervals as required by the independent claims 7 and 8. Attention is called to column 3, lines 16 – 23 of Hayashi wherein it is stated:

> Upon completion of the processing operation, an interruption factor resetting operation is carried out(Step S3). A plurality of interruptions may occur at the same time, or during the routine another interruption may occur. Therefore, in step S4 it is determined whether or not any interruptions is still available. **When an interruption is available step S1 is effected again**, and the corresponding processing operation is carried out. (Emphasis added)

Also, as shown in the flow chart of Fig. 2, in the event that there is positive result at step S4, interrupts will continue to be permitted, while in the even of a negative result (i.e. there are no other interruptions), it is clear that the interruption process will cease at least for a time while the program loops back to step S1. This will most certainly cause the time between interrupts to vary sporadically.

The claimed subject matter set forth in claims 7 and 8 as per the proposed amended, is not therefore anticipated by the disclosure of Hayashi. Entry of these amendments is deemed proper in that they clarify over the Hayashi reference and those discussed below, and thus render the claims over the cited art.

2) The rejection of claims 2-5 and 7-8 under 35 USC § 102(b) as being anticipated by Yonezawa et al. is respectfully traversed.

It is again submitted that rejections under the 35 USC § 102 statute, are based on the premise that to anticipate a claim, each and every element of the claim must be shown in a single reference. When a claimed element cannot be found in the reference, the reference does not anticipate the claimed invention. Further, it is incumbent upon the Examiner to identify in the rejection where in the reference each element may be found. Ex parte Levy, 17 U.S.P.Q.2d 1461 (Bd. Pat. App. Intrf. 1990). Consequently, when a rejection fails to identify a claimed element, the rejection fails to establish a *prima facie* case of anticipation.

Again, in this rejection, none of the claimed memories are identified and there is no indication of where the claimed memories are disclosed in the Yonezawa et al. reference. It is respectfully submitted that the rejection is untenable for at least this reason.

In this rejection element 24 is cited as being the claimed interrupt trigger generating means. However, this interrupt generating circuit 24 operates in response to a power supply cut-off detecting circuit 21, high temperature abnormality detecting circuit 22, and software abnormality detecting circuit 23. It cannot, therefore, cannot be expected to generate interrupt triggers with the timing as set forth in the pending independent claims. Further, it is the abnormality generation interrupt processing that is executed in response to the interrupt generating circuit 24 as an interrupt, and not peripheral service process as per the claimed subject matter.

In connection with claims 2 and 3 it the rejection states that Yonezawa et al. is such that the "interval" or predetermined time can be set or changed by a "timer." However, in this instance the "timer" is not identified and the suggestion that the time can "set or changed" by a timer would seem more fitting to a rejection under § 102 inasmuch as there is no disclosure of this setting or changing identified.

A review of Yonezawa et al. indicates that Fig. 15 discloses a timer T which is connected to an "execution right changeover processing unit" ES. However, column 11, lines 26 – 67 of Yonezawa et al. discloses:

As shown in the example of FIG. 15, the first step of sequence control processing SQ is to execute a load command LD. Subsequently, the execution moves to an AND command, an OR command, and an output command (OUT), at which time 10 ms passes. Then, a time-up signal is transmitted as an interrupt signal from timer T to execution right change-over processing unit ES. CPU 1 inputs this interrupt signal, **but at this time the control executing right is still held by BPU 2. As a result, CPU 1 is unaffected by this time-up interrupt**.

The sequence processing further advances, and BPU 2 executes load command LD. By the time the next 10 ms time-up interrupt signal is transmitted, the control executing right has been handed over to CPU 1 for execution of application command (1). Consequently, execution right change-over processing unit ES changes the processing which is to be executed by CPU 1 from sequence processing SQ to BASIC processing BAS. Thus, CPU 1 starts processing BASIC processing program BAS in accordance with task scheduler TS. Execution of sequence control processing SQ remains stopped.

Thereafter, timer T is again brought into a time-up state, and another 10 ms interrupt signal is generated. At this time, execution right change-over processing unit ES in CPU 1 temporarily stores the present conditions of the BASIC program (e.g., values of registers, value of a program counter, etc.) in data memory 7 (shown in FIG. 11), and causes the operation of sequence control processing SQ, which had been stopped, to resume.

> When execution of sequence control processing SQ is completed, sequence control processing SQ transmits a notice of completion to execution right change-over processing unit ES, **irrespective of whether a time-up signal has been issued, and CPU 1 initiates or resumes execution of BASIC processing BAS**.
>
> In sum, the system operates by alternating execution of sequence control processing SQ and BASIC processing BAS every 10 ms **while CPU 1 has the execution right**. As a result, sequence processing SQ and BASIC processing BAS appear to the user as if they were being executed simultaneously. Hence, multi-processing is practicable. (Emphasis added)

This disclosure makes it clear that an interrupt signal can, with the Yonezawa et al. arrangement, be issued, however, depending on execution rights, the interrupt can be ignored, and/or CPU 1 can resume execution of BASIC processing irrespective of the time-up signal (interrupt) being issued.

Further, as will be appreciated, timer T is set to switch at the end of a predetermined interval which can be set depending on the system configuration. This can be 10 ms(see column 11, lines 21-25). However, this means that, given that the system actually responded to the interrupts and did not ignore them under given circumstances, that the prescribed amount of time and the prescribed interval would be the same. As will be noted, the above proposed amendments are such as to distinguish over this feature by calling for these periods to be unequal in duration.

Therefore, the subject matter of claims 7 and 8 as amended above, cannot be met by the disclosure of Yonezawa et al. It is submitted that the claimed subject matter is patentable over the disclosure of Yonezawa et al. for at least the reasons advanced above.

3) The rejection of claims 2-5 and 7-8 under 35 USC § 102(b) as being anticipated by Flood et al. is respectfully traversed.

Flood et al (U.S. patent No. 5,139,189) disclose a programmable controller configured to execute several priority levels of program tasks. According to column 2, lines 16-25, Flood et al. allocate the amount of processing time devoted to the machine operation control program and the amount of time devoted to executing background tasks. However, referring to the same portion, as a method of resolving such, background tasks (arguably equivalent to the peripheral service process of the present invention) are executed in a time slice manner without adversely interfering with the execution of the control program. As it is apparent from such disclosure, Flood et al. merely execute the peripheral service process in a time slice manner. Such a technique is equivalent to the prior art technique described in the instant specification.

Therefore, Flood et al. only disclose executing peripheral service process in a time slice manner. It does not disclose or suggest ensuring the cyclic execution of a peripheral service process by a prescribed constant amount of time every time an interruption trigger is generated at a predetermined interval which is different from the prescribed amount of time, while the user program process and the I/O refresh process are executed by the microprocessor according to the normal procedure.

Flood at column 22, line 61 – column 23, line 3, discloses:

> Interrupt routines allow high priority operations to be executed upon the occurrence of a given event and comprise processor input interrupts (PII) and selectable timed interrupts (STI). Processor input interrupts are started by an externally generated input. To accommodate the processor input interrupts, each program execution module 18 has an interrupt interface 99 (FIG. 4) which receives and handles interrupt signals from external devices. **The selectable timed interrupt**

routines are started at regular user specified intervals by the system's real time clock. (Emphasis added)

It is therefore clear that the proposed claimed requirement that the prescribed intervals and the prescribe amount of time are unequal in duration, cannot be met by this arrangement.

Further, in connection with the disclosure of time slice, assume that there are, merely by way of example, three tasks A, B and C. With this assumption assume for the sake of discussion that the execution order and the execution time for each task is:

Task A 3ms

Task B 2ms

Task A 1ms

Task C 1ms

Task B 1ms

The execution time (duration) of each task is performed for a prescribed amount of time according to a timer, and upon expiation of the prescribed amount time, a switch to another task is induced. However, it is not determined to which task the switch is made to. In addition, the time period for the execution of a task (execution duration) is set and another task is executed upon completion of the previous task for the amount of time that is set for that task. It is therefore submitted that the Flood et al. reference does not disclose or suggest in the manner required by the claim amendments.

In connection with claim 5, the rejection states that it is clear from Flood et al. that the so called "prescribed interval" or selectable time is the time it takes to finish the peripheral service process plus the predetermined time for another interruption operation. However, if the selectable time is the time it takes to finish the peripheral service process, and the peripheral service process must be expected to vary from the run to run, then this time plus that for an interrupt must be a variable and thus quite different from the proposed amendments to the claims.

This rejection is also traversed in that each of the claimed elements has not been identified in the manner required and it is therefore not clear on the record if the Flood et al. reference actually discloses all of the claimed subject matter.

4) The rejection of claims 2-5 and 7-8 under 35 USC § 102(b) as being anticipated by Shultz et al. is respectfully traversed.

Shultz (U.S. patent No. 4,638,452) discloses a programmable controller including a main processor which can be interrupted by a support processor which operates as a real time clock. According to this programmable controller, the interval between interrupts is determined by instructions within the user control program, and is disclosed in the abstract as being dynamically altered as required.

Column 10, line 66 to column 11, line 12, of Shultz et al. disclose:

> Because both the real time interrupt rate and the interrupt routine which is executed in response to each interrupt are controlled by the user, the preferred embodiment of the invention also includes means for **insuring that enough time is allowed for the normal programmable controller functions to be performed**. When the length of time **required to execute the interrupt routine** exceeds a preestablished portion of the time interval between interrupts, the **interrupt time interval is changed**. As described above, when the execution of the user's interrupt routine exceeds two-thirds of the user's programmed interrupt time interval, the system waits for an entire interrupt time interval after the completion of the user's interrupt routine before producing another real time interrupt. (Emphasis added)

Thus, as will be appreciated Shultz clearly teaches away from having constant set periods/amount of time and doe not discloses of suggests the execution of a peripheral service process as set forth in the independent claims as proposed above.

The dependent claims are also patentable for at least the same reasons as the independent claims on which they depend. In addition, they recite additional patentable features when considered as a whole.

This rejection is also traversed in that each of the claimed elements has not been identified in this rejection in the manner required and it is therefore not clear on the record if the Shultz et al. reference actually discloses all of the claimed subject matter.

Conclusion

In conclusion, it is submitted that the claimed subject matter is patentable over the references which have been applied. Favorable reconsideration and allowance of this application is courteously solicited.

Respectfully submitted,

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By

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